1 **WHAT IS CLAIMED IS:**

1   1.   A method for recording segment execution times in a processing system,
2 the method comprising the steps of:
3   recording a timestamp corresponding to the beginning of a segment to be
4 executed, the recording step being conducted through a firmware operation; and
5   updating the timestamp with an elapsed segment execution time, the updating step
6 being conducted through a plurality of hardware based operations, wherein the plurality of
7 hardware based operations are executed without firmware interaction.

1   2.   The method of claim 1, wherein the recording step comprises writing a first
2 memory address into a globally accessible timestamp address register.

1   3.   The method of claim 1, wherein the updating step comprises:
2   reading the contents of a second memory location designated by an update address
3 register;
4   writing the contents of the second memory location into a location value register;
5   adding the elapsed segment execution time to the location value register contents;
6 and
7   storing the location value register contents to the second memory location
8 indicated by the update address register.

1   4.   The method of claim 3 further comprising the steps of:
2   clearing the elapsed segment execution time stored in an elapsed time register; and
3   setting a second value in the update address register with a first value from a
4 timestamp address register.

1   5.   The method of claim 1 further comprising the step of initializing hardware
2 components of the processing system, the initializing step further comprising the steps of:
3   disabling timestamp assist functions;
4   setting an elapsed time register to an initial value;
5   writing an initial address into a timestamp address register;
6   writing the initial address to an update address register; and
7   enabling the timestamp assist functions.

1   6.   The method of claim 1 further comprising the step of invoking an interrupt handler
2   if a second segment is received for processing during the updating step.

1   7.   The method of claim 6, wherein the step of invoking an interrupt handler further
2   comprises:
3   generating an interrupt signal in a memory controller;
4   determining if the updating step is still in process;
5   determining if a timeout has been reached if the updating step is determined to still
6   be in process;
7   restarting the updating step for the second segment; and
8   clearing the interrupt signal from the memory controller.

1   8.   A method for recording segment execution times through a central processing
2   unit, the method comprising the steps of:
3   writing a first determined memory address into a timestamp address register with a
4   firmware based operation;
5   reading contents of the first determined memory address into a location value
6   register with a hardware based operation;
7   adding an elapsed time value corresponding to a segment execution time to the
8   contents read into the location value register to create an updated value, the adding step
9   being conducted with a hardware based operation; and
10   storing the updated value to the first determined memory address with a hardware
11   based operation.

1   9.   The method of claim 8, wherein the reading step comprises:
2   reading a memory location from an update address register in a timestamp assist
3   logic module; and
4   writing the memory location into the location value register in the timestamp assist
5   logic module.

1   10.   The method of claim 8, wherein the adding step comprises:
2   reading the elapsed time value from an elapsed time register in a timestamp assist
3   logic module, the elapsed time value corresponding to an elapsed time between a start of a

4   segment execution and the step of reading the elapsed time; and

5   adding the elapsed time value to the contents stored in the location value register.

1   11.   The method of claim 8, wherein the storing step comprises:

2   reading the contents of a location value register; and

3   writing the contents read from the location value register to the first determined.

1   12.   The method of claim 8 further comprising the steps of:

2   generating a segment processing interrupt when a second segment is received for

3   processing during one of the writing, reading, adding, and storing steps;

4   transmitting the segment processing interrupt to a processor;

5   interrupting segment processing; and

6   invoking a timestamp busy interrupt handler.

1   13.   The method of claim 12, wherein invoking the timestamp busy interrupt handler

2   comprises:

3   determining if the updating step is still in process;

4   determining if a timeout has been reached if the updating step is determined to still

5   be in process;

6   restarting the updating step for the second segment; and

7   clearing the interrupt signal from the memory controller.

1   14.   An apparatus for recording segment execution times in a processing system, the

2   apparatus comprising a memory controller in communication with a central processing

3   unit and a memory, the memory controller comprising:

4   at least one control register;

5   at least one address register; and

6   a timestamp assist logic module,

7   wherein the memory controller is configured to conduct timestamp update

8   operations autonomously from the central processing unit.

1   15.   The apparatus of claim 14, wherein the timestamp assist logic module comprises:

2   an elapsed time module;

3   an update address register; and

4   a location value register.

1   16.   The apparatus of claim 15, wherein the elapsed time module comprises an elapsed

2   time register having an updated elapsed time value stored therein.

1   17.   The apparatus of claim 14 further comprising:

2   a processor bus in communication with the central processing unit and the

3   memory controller for communication therebetween;

4   a memory bus in communication with the memory and the memory controller for

5   communication between the memory controller and a plurality of memory locations in the

6   memory; and

7   a system bus in communication with the memory controller, the system bus being

8   configured to connect one or more additional devices to the memory controller.

1   18.   The apparatus of claim 14, wherein the control register is configured to generate

2   an interrupt signal when the timestamp assist module receives a second segment for

3   processing while a first segment is currently processing, the interrupt signal being

4   transmitted to the central processing unit via a system bus.

1   19.   A memory controller for recording segment execution times in a complex

2   processor system, the memory controller comprising:

3   a timestamp assist logic module;

4   a timestamp control module;

5   a timestamp address module; and

6   wherein the memory controller is configured to communicate with a memory in

7   order to execute a timestamp update operation corresponding to a particular segment

8   execution time, the timestamp update operation being conducted without interaction with

9   an operating system of the complex processing system.

1   20.   The memory controller of claim 19, wherein the timestamp assist logic module

2   comprises:

3   an elapsed time module;

4   an update address module; and

5   a location value module.

1   21.   The memory controller of claim 20, wherein the elapsed time module comprises a

2   device for calculating and storing an elapsed time value corresponding to the time elapsed

3   between initial segment execution and completion of segment execution.

1   22.   The memory controller of claim 20, wherein the elapsed time module comprises an

2   elapsed time register having an updated elapsed time value stored therein.

1   23.   The memory controller of claim 19 further comprising:

2   a processor bus in communication with the operating system and the memory

3   controller for communication therebetween;

4   a memory bus in communication with a plurality of memory locations in the

5   memory and the memory controller for communication therebetween;

6   a system bus in communication with the memory controller for communication

7   between the memory controller and additional devices in the complex processing system.

1   24.   The memory controller of claim 19, wherein the timestamp control module is

2   configured to generate an interrupt signal when the timestamp assist logic module receives

3   a second segment for processing while a first segment is currently processing, the interrupt

4   signal being transmitted to a central processing unit.